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Effect of Contact between Electrode and Interconnect on Performance of SOFC Stacks

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Abstract

This work investigates the effect of contact between electrodes and alloy interconnects on output performance of solid oxide fuel cell (SOFC) stacks. The measured maximum output power density (p_{max}) of the unit cell increases from 0.07 to 0.1 W cm^{-2} by increasing the tip area of the interconnect from 40 to 60 cm^2. The p_{max} increases from 0.07 to 0.15 W cm^{-2} upon the addition of nickel foam and Ag mesh on the anode and cathode side, respectively. An additional $(La_{0.75}Sr_{0.25})_{0.95}MO_{3-\sigma}$ cathode current collecting layer is re-printed on the original cathode current collecting layer, which aims to further improve the performance of the stack and individual cell. The performance of a 3-cell short stack assembled by the cells with a new cathode current collecting layer is evaluated by measuring the current–voltage curve. The results indicate that the p_{max} values of the stack and individual cells are enhanced from 0.07 to 0.37 W cm^{-2} and 0.15 to 0.5 W cm^{-2} at 850 °C, respectively. The performance of the whole stack and individual cells is greatly improved due to the interconnect embedded in the re-printed new cathode current collecting layer.

Keywords: Cathode Current Collector, Contact, Power Density, Stack, Solid Oxide Fuel Cell

1 Introduction

The main components of a typical planar solid oxide fuel cell (SOFC) stack are metal interconnectors, seal materials and unit cells [1, 2]. The output performance of the SOFC stack is determined by the resistance of the metal interconnector, the unit cell and the interface contact between components. The resistance of the metal interconnect is relatively small at the operating temperature of 700–850 °C, and the performance of a single cell is decided generally by chemical composition and fabrication processing [3]. The resistance of interface contact between the components is related to the effective contact area, which usually refers to the contact between interconnects and electrodes of a single cell. Recently, the interface contact between the metal interconnect and the electrode has been investigated by experimental methods and theoretical analysis, respectively [4–7]. It was found that the area specific resistance (ASR) of the unit cell decreased from 1.43 to 0.19 Ω cm^2 at 800 °C when the effective contact area was increased from 4.6% to 27.2% by adding silver or platinum mesh on the cathode side [6]. The output power of the single cell was investigated by adding platinum paste, platinum net, stainless steel (SUS) mesh and $LaN_{i0.6}Fe_{0.4}O_3$ (LNF) powder on the cathode side. The results indicated that the cell performance is increased more than six times upon the addition of precious metals than that of direct contact between the interconnect and electrode [7]. Furthermore, an empirical numerical model established by Lynch and Liu [8] suggests that decreasing the resistance between components in cell testing is crucial. Therefore, the measured performance of the unit cell is related to the contact area. However, the output performance of the stack is poor even when Pt or Ag mesh is added on the cathode side. In addition, the obtained average power density of the single cell in the stack is still much lower than the cell tested itself in previous publications [1, 2, 9]. Herein, it is considered that the essential factor on the output performance of the stack and individual cells is still not clear. This study aims to reveal the

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essential effect of the stack and individual cells on output performance by designing contact between the components and the cathode current collecting layer. The optimal contact method between components for SOFC stack will be determined.

2 Experimental Procedures

Typical anode-supported SOFCs composed of Ni-Y_2O_3 stablised ZrO_2 (YSZ)/YSZ/$(La_{0.75}Sr_{0.25})_{0.95}MnO_{3-\delta}$ (LSM) were manufactured at the Ningbo Institute of Material Technology and Engineering, China. The total area of the cell used to assemble the stack was 13 × 13 cm^2 with an active area of 10 × 10 cm^2. The preparation process and other parameters of the unit cell were described elsewhere [10]. The stack consists of Fe-16Cr alloy interconnects, Ni-YSZ/YSZ/LSM unit cells, sealing glass and metal meshes or nickel foams. Nickel wires were used as a voltage probe. To investigate the effect of interface contact on the output performance of the stack, the stack was assembled according to the configuration demonstrated in Figure 1.

As shown in Figure 1, six different contact modes between the interconnect and the unit cell were implemented in this study, which included: (A) for cell 1, direct contact of electrode with interconnect-A; (B) for cell 2, nickel foam added on the anode side, and the cathode directly contacting with interconnect-A; (C) for cell 3, nickel foam on the anode side and silver mesh on the cathode side; (D) for cell 4, nickel foam on the anode side and stainless steel (SUS 430) mesh on the cathode side; (E) for cell 5, nickel foam on the anode side, and the cathode barely contacting with interconnect-B; (F) for cell 6, the two electrodes nakedly contacting with interconnect-B. The tip area of interconnect-A and interconnect-B is 40 and 60 cm^2, respectively.

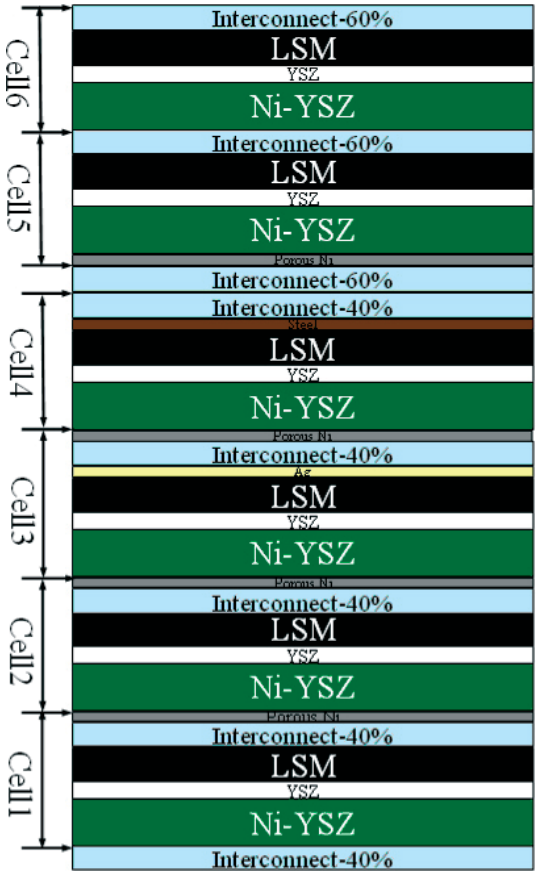

Fig. 1 Schematic diagram of the interface contact between components of an SOFC stack.

An additional layer of $(La_{0.75}Sr_{0.25})_{0.95}MnO_{3-\delta}$ (LSM2) particles with a diameter of approximately 75 μm was coated on the original cathode side (LSM1) to further improve the output performance of the stack and individual cells, as shown in Figure 2. The 3-cell short stack was then assembled using the single cells with LSM2, in which the nickel foam was placed on the anode side, and the cathode side was directly adhered to interconnect-A. To investigate the individual effect of LSM1, LSM2 and contact between components on the output performance of unit cell, nickel slices (W_1, W_2) with a thickness of approximately 10 μm were pasted on the surface of LSM1 before coating LSM2, while nickel slices W_0 was pasted on the cathodic side of interconnect, W_3 on the anode surface, and W_4 on the LSM2 surface.

Following assembly, the stack was placed in a furnace and heated to 850 °C with a heating rate of 1 °C min^{-1}. An external weight was loaded on the stack for better sealing. The hydrogen (H_2) was then fed into the stack for anode reduction. After reduction for 5 h, the performance of the stack was tested with pure H_2 as fuel and air as cathode gas.

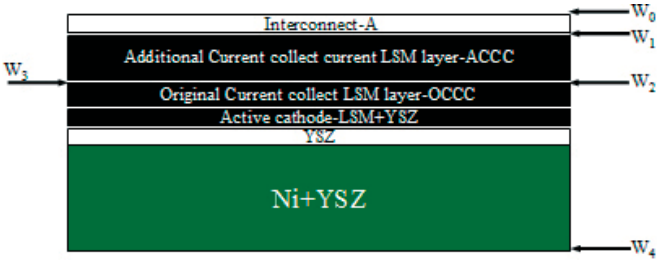

Fig. 2 Schematic demonstration of the locations of the nickel slices.

3 Experimental Results and Discussions

The current–voltage (*I*–*V*) curve of the 6-cell stack is shown in Figure 3(a), and the output performance of the individual cells is given in Figure 3(b). The maximum power density (p_{max}) of the stack is 0.07 W cm^{-2} when feeding pure H_2 into anode at a flow rate of 8.3 sccm cm^{-2} and air into cathode at 16.7 sccm cm^{-2}. The p_{max} reached 0.15 W cm^{-2} for the cell with nickel foam as the anodic current collector and silver mesh as the cathodic current collector (cell 3). Other five unit cells of the stack can only obtain a p_{max} of 0.07–0.1 W cm^{-2} for other five current collecting modes. It is clear that the measured cell performance can be arranged from low to high according to the following sequence: $P_{cell\ 1} < P_{cell\ 6} < P_{cell\ 4}$

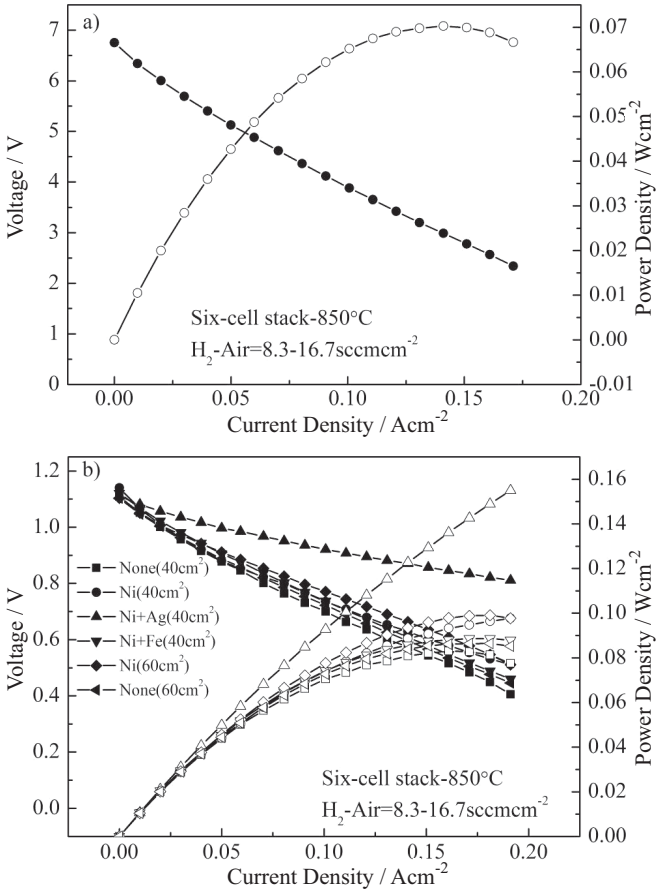

Fig. 3 *I–V* curves for (a) the 6-cell stack and (b) individual cells within the stack.

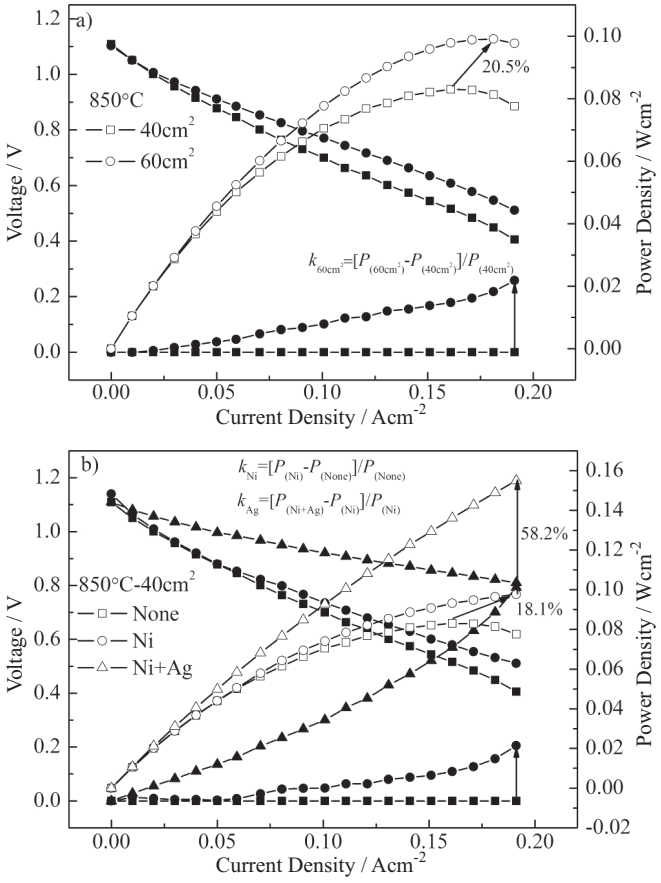

Fig. 4 *I–V* curves for the unit cell within a stack having (a) different contact area and (b) different contact interfaces.

$< P_{\text{cell 2}} < P_{\text{cell 5}} < P_{\text{cell 3}}$. The output performance of cell 4 in the stack is higher than that of cell 2 or cell 5, which may result from the increasing resistance of the SUS430 mesh.

Figure 4(a) shows the output performance of the unit cell having different contact area between the interconnects and electrodes. The difference rate (k) for cell performance improvement can be defined by the following equation:

$$k = \frac{P_{60\,\text{cm}^2} - P_{40\,\text{cm}^2}}{P_{40\,\text{cm}^2}}$$

It can be seen that the cell output power increases parabolicly upon the increasing contact area, and the peak value of k reaches 20.5% when the tip area of interconnect is increased from 40 to 60 cm^2. Figure 4(b) represents the *I–V* curves of the unit cell under various contact conditions. Compared to the performance of the cell with electrode directly adhered to interconnect-A (cell 1), the $p_{\max}$ at 850 °C is increased by 18.1% upon adding nickel foam on the anode side and 58.2% by adding Ag mesh on the cathode side, respectively.

It is clear that the output performance of the cell in the stack is improved greatly by adding Ag mesh on cathode side. The Ag mesh placed on cathode side can increase the contact area between the interconnect and the cathode, which improves the output performance of the unit cell in the stack. In this study, however, the unit cell still shows moderate performance after adding the auxiliary metal current collecting layers onto both electrodes. Typical microstructure of the unit cell in the 6-cell stack is shown in Figure 5(a). The cell has a double cathodic layer consisting of approximately 30 µm of LSM active layer and approximately 100 µm of cathode current collecting layer (i.e. LSM1). The particle size of LSM1 is approximately 0.5 µm. The cell can obtain a $p_{\max}$ of ~0.6 W cm^{-2} when subjected to single cell testing, which is much higher than the $p_{\max}$ of the unit cell in the 6-cell stack. It is known that the cell performance with a fabrication of Ni-YSZ/YSZ/LSM can be enhanced by improving the current collecting layer [7]. Hence, the LSM1 configuration is expected to be optimised to considerably improve the performance of the unit cell and the whole stack. A new current collecting layer mode (i.e. LSM2) is designed by spraying the spherical LSM powder with a much larger diameter onto the LSM1, as shown in Figure 5(b). The particle size of the cathode current collecting layer is increased from nanometer to micrometer and the thickness of the LSM2 is also approximately 100 µm.

The performance of the 3-cell stack with LSM2 is shown in Figure 6(a). The $p_{\max}$ of the stack reaches 0.28, 0.34 and 0.37 W cm^{-2} at 750, 800 and 850 °C, respectively. Figure 6(b)

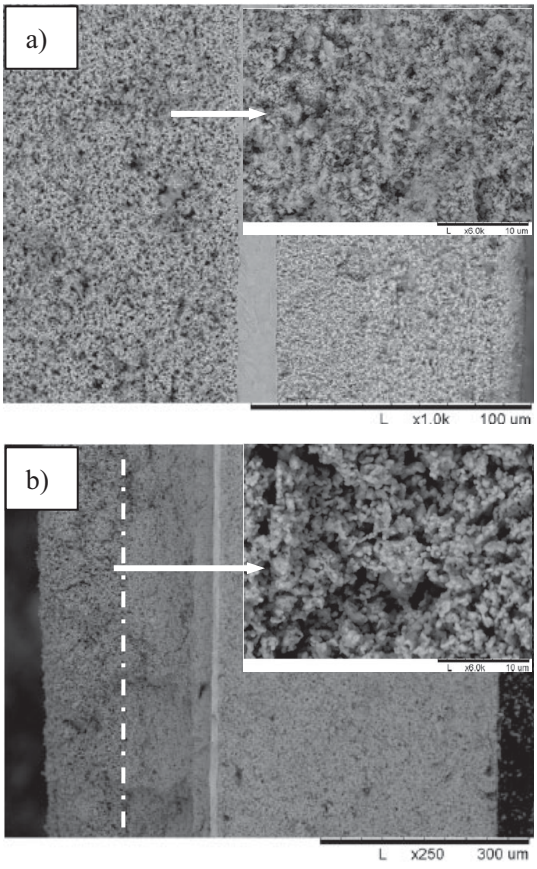

Fig. 5 Microstructure of the unit cell within (a) 6-cell stack and (b) 3-cell stack.

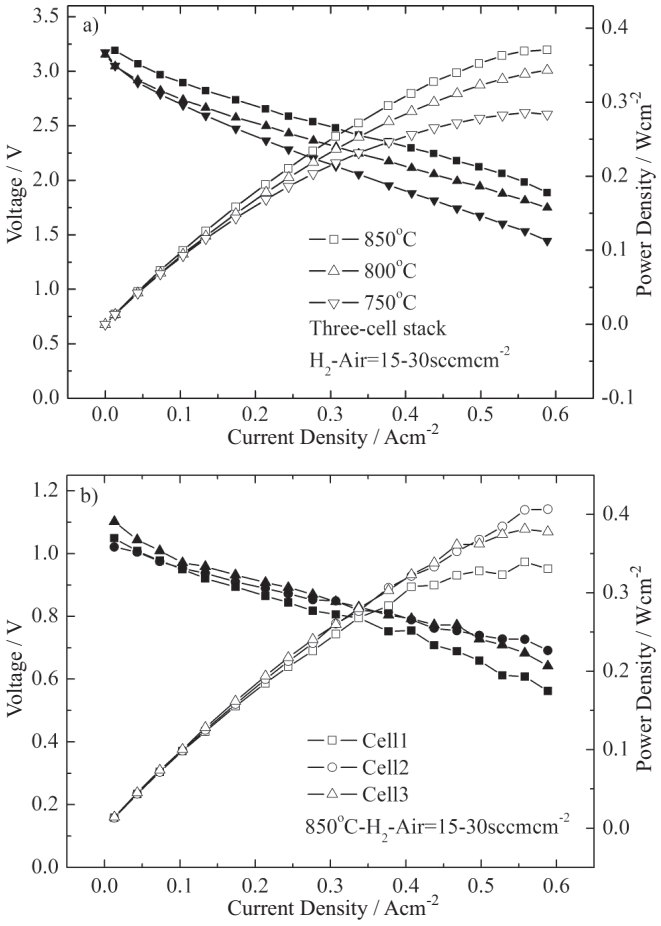

Fig. 6 *I–V* curves of (a) the 3-cell stack and (b) individual cell within the stack.

shows the *I–V* curves of the unit cells at 850 °C, and the p_{max} of the unit cell achieves more than 0.4 W cm^{-2}. This p_{max} value is 3 times more than that obtained from the forthmentioned 6-cell stack at 850 °C. It can thus be concluded that the output performance of the stack and the individual cell can be tremendously enhanced by changing the current collecting layer on the cathode side, which is consistent with the previously reported results [11].

Figure 7 shows the *I–V* curves obtained from various locations on cell 2 in the 3-cell stack, where $p_{W_1W_4}$ refers to the testing results between W_1 and W_4, $p_{W_2W_4}$ and $p_{W_3W_4}$ arise from W_2, W_3 and W_4, $p_{W_1W_0}$ stems from W_1 and W_0. As can be seen from Figure 7, the $p_{W_2W_4}$ and $p_{W_3W_4}$ yield the highest output performance among different locations of the unit cell.

The output performance from $p_{W_2W_4}$ is nearly equal to that from $p_{W_3W_4}$, indicating that the voltage loss in different locations on the same horizontal cathode or anode layer is equivalent. The output performance from $p_{W_1W_4}$ nearly equals to that from $p_{W_0W_4}$, indicating that the resistance of the interconnects and the contact resistance between cathode and interconnect is negligible. Improvement of the LSM1 not only reduces the interface contact resistance, but also further increases the overall cell output performance.

The surface traces on the cell cathode and interconnect of the 6-cell stack and the 3-cell stack are shown in Figure 8.

Some regular columniform craters can be found on the surface of the cathode and interconnect. Clearly shallow traces exist on the cell cathode surface left by the interconnect tip after testing the 6-cell stack, as shown in Figure 8(a). The deep and legible craters are observed in the contact sites of the cathode and interconnect for the 3-cell stack as shown in

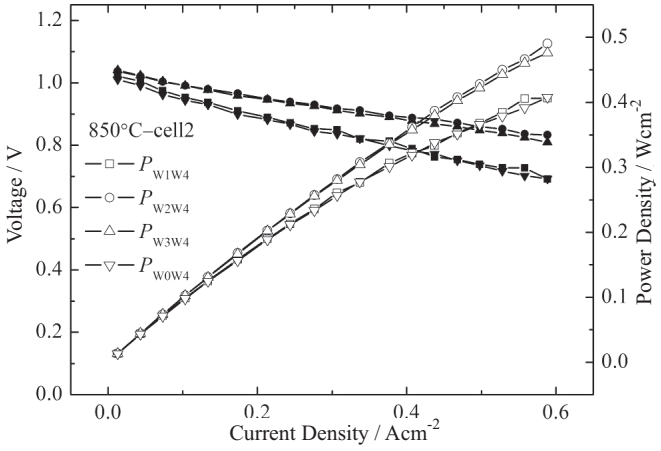

Fig. 7 *I–V* curves of cell 2 within the 3-cell stack tested at different locations.

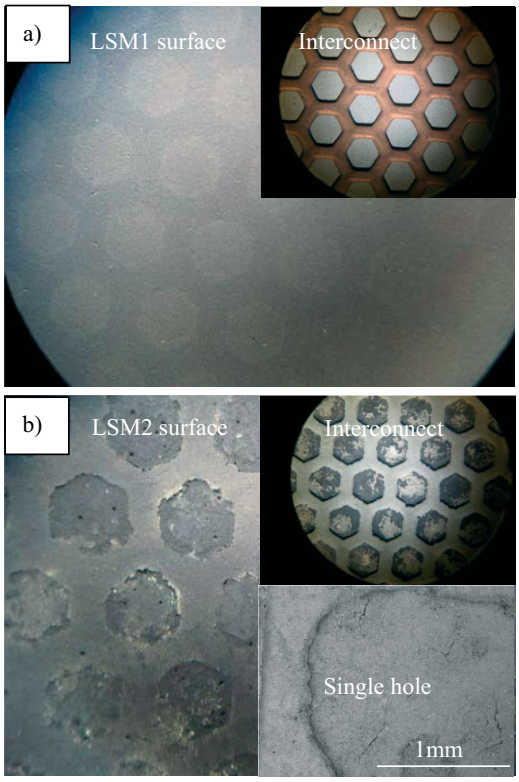

Fig. 8 Surface morphology of contact interfaces between a cell and interconnect for: (a) 6-cell stack and (b) 3-cell stack.

Figure 8(b). The immersion depth of the holes in Figure 8(b) is approximately 0.1 mm. The contact area between the cathode and interconnect for the 3-cell stack is only increased by 37.1% by comparison with the contact area for the 6-cell stack. Jiang et al. [6] reported that the p_{max} increased from 0.3 to 0.52 W cm^{-2} when the designed contact area between the cathode and Ag mesh is increased from 5.34% to 27.2%. Obviously, the increase of contact area can effectively enhance the cell output performance. However, the increasing ratio of the cell output performance is much less than that of contact area. Liu et al. [12] indicated that reducing craters on the surface of the electrolyte left by LSM grains can degrade the cell performance, which also resulted from decreasing the contact area between the electrolyte and cathode. However, the output performance of the stack in this study is increased by more than five-fold by adding LSM2, whereas the contact area between the components is only increased by 37.1%. The increasing ratio of the stack output performance is approximately 10 times larger than that of the contact area. It can be concluded that the increasing output performance may not only determined by increasing the contact area.

It is well known that the output performance of the unit cell in the stack is determined by the resistance of the unit cell, the interconnect and the voltage loss arising from contact between the two components. The voltage drop is partially attributed to the contact between the interconnect and the electrode. The bad interface contact increases the difficulty in transferring electrons and interrupts the electrochemical reaction in the SOFCs. Therefore, there may be a large part of electrons produced from hydrogen in the active anode that move irregularly resulting from poor contact interface, while other electrons transfer directly through the contact interface from the interconnect to porous active cathode layer where oxygen reacts, as shown in Figure 9(a). It can be concluded that there are not enough electrons provided to the oxygen reaction for the poor-contacted cell, causing poor output performance. Contrary to the above deduction, more electrons transfer directly through the contact interface from interconnect to active cathode layer as the interconnect tips immerse into the cathode current collecting layer, as shown in Figure 9(b). Therefore, the oxygen reduction reaction in the cathode triple-phase boundaries has more electrons from the interconnect, causing a substantial increase in cell performance.

The metal interconnect tip can easily immerge into the soft structure after coating the LSM1 by LSM2, thus leading to negligible contact resistance between interconnect and cathode surface and significant improvement in the cell output

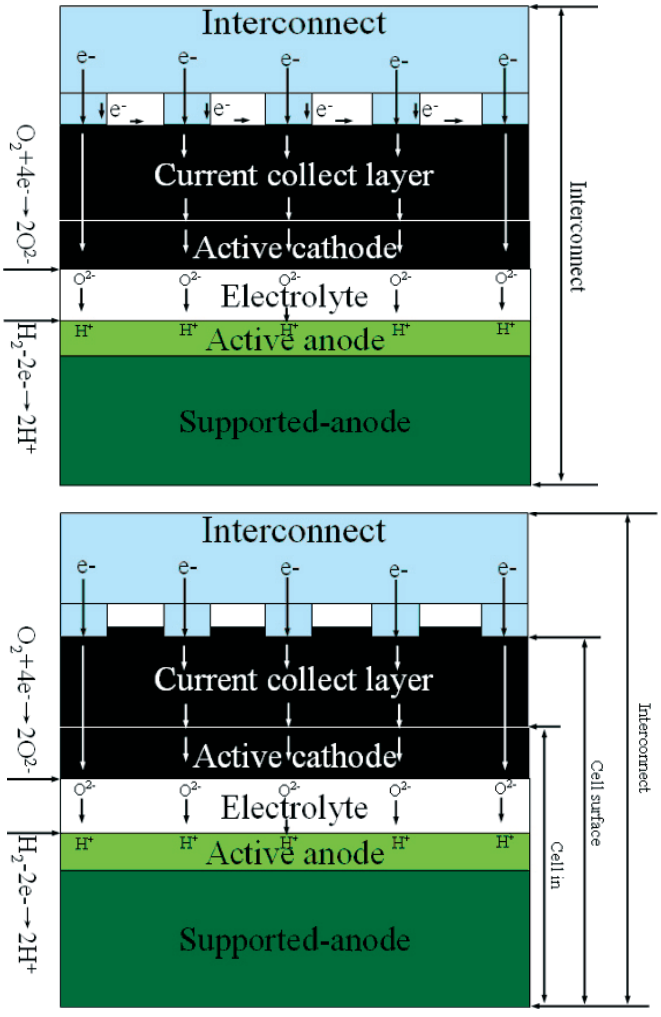

Fig. 9 Schematic demonstration of electronic transfer in a repeat unit within a stack having (a) surface contact and (b) immersed contact.

performance. The output performance of the unit cell may increase more with increasing immersion depth of the interconnect tip into the cathode current collecting layer. This suggests the contact between the cell and interconnect is not a two-dimensional issue concerning only the interface plane between the cell and interconnect, but a three-dimensional issue involving both the interface plane and the depth of the interconnect tip into the cell, specifically the cathode current collecting layer. Therefore, increasing the contact between the interconnect and the cathode layer in the depth direction can improve the output performance of the stack and the individual cell sharply. The increasing ratio is much larger than that from increasing the contact area on the interface plane between components.

4 Conclusion

The p_{max} of the unit cell increased by 20.5% after increasing the contact area from 40 to 60 cm^2 between the metal interconnect and electrode. Compared to the output performance of the unit cell having direct contact between electrodes and interconnects, the p_{max} increased by 18.1% and 58.2% by adding nickel foam and Ag mesh onto anode and cathode, respectively. The p_{max} of the stack and individual cell increased from 0.07 to 0.37 W cm^{-2} and 0.15 to 0.5 W cm^{-2} at 850 °C by spraying a new soft layer with coarse $(La_{0.75}Sr_{0.25})_{0.95}MO_{3-\sigma}$ cathodic powder on the original cathode current collecting layer. The tip of interconnect easily immersed into the fluffy structure of the new cathode current collecting layer, which greatly improved the contact between the interconnect and the cathode current collecting layer, thus significantly increased the output performance of the unit cell and the stack for planar SOFCs.

Acknowledgements

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